[0015] In the drawings, reference characters which are the same denote similar elements throughout the several views:

[0016] FIG. **1**A is a block diagram of one embodiment of an AFCI system;

[0017] FIGS. **1**B through **1**H are schematic layouts of wiring schemes that can each be used with any one of the embodiments of FIGS. **1**A, **3**A, **3**B, **3**C, and **3**E;

[0018] FIG. **2**A is a cross-sectional view of a conductive path comprising a line side phase and a line side neutral;

[0019] FIG. **2**B is a cross-sectional view of a conductive path comprising a line side phase and a line side neutral with one conductive path being disposed concentric with respect to the other conductive path;

[0020] FIG. **2**C is a plan view of a first configuration of sensors for use in any of the embodiments herein disclosed;

[0021] FIG. **2**D is a transparent plan view of a second configuration of sensors for use in any of the embodiments herein disclosed;

[0022] FIG. **2**E is a plan view of a third configuration of sensors for use in any of the embodiments herein disclosed;

[0023] FIG. **2**F is a side cross-sectional view of an arrangement which includes a current sensor, a high frequency sensor, and a differential sensor;

[0024] FIG. **3**A is a circuit diagram of an embodiment of an AFCI system;

[0025] FIG. **3**B is a circuit diagram of another embodiment of an AFCI system;

[0026] FIG. **3**C is a circuit diagram of another embodiment of an AFCI system;

[0027] FIGS. **3**D through **3**F are detailed views of portions of FIG. **3**C;

[0028] FIG. **4**A is a flow chart for the process for determining a series arc;

[0029] FIG. **4**B is a flow chart for the process for determining a parallel to ground arc;

[0030] FIG. **4**C is a flow chart for the process for determining a parallel to neutral arc;

[0031] FIG. **4**D is a simplified flow chart of an embodiment of the process performed by the AFCI system;

[0032] FIG. **5**A is a graphical depiction of an electrical signal on a line;

[0033] FIG. **5**B is a graphical depiction of a reading and calculation of values obtained from the electrical signal on the line with this reading being performed across at least two time periods;

[0034] FIG. **5**C is a graphical depiction of multiple time period of FIG. **5**B;

[0035] FIG. **5**D is a graphical depiction of a first duration of recording time period for determining an arc;

[0036] FIG. **5**E is a graphical depiction of a second duration of recording tie period for determining an arc;

[0037] FIG. **5**F is a graphical depiction of a third duration of recording time period for determining an arc;

[0038] FIG. **6**A is a perspective view of one embodiment of a component layout for the AFCI system;

[0039] FIG. **6**B is a side view of one embodiment of a component layout of the sensors with respect to a circuit board;

[0040] FIG. **7** is a front perspective view of a housing for an AFCI system.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0041] FIG. **1**A depicts a block diagram for one embodiment of an arc fault circuit interrupter (AFCI) device **5**. At least one embodiment of the invention relates to an AFCI system **5** which can be disposed inside of an enclosure such as a single-gang enclosure. The AFCI system **5** can include a current path comprising a phase conductive path having a line side and a load side, and a neutral conductive path having a line side and a load side.

[0042] FIG. **1**A includes one embodiment of a wiring scheme layout **110**. Alternatively, any wiring scheme layout depicted in FIGS. **1**B-**1**H may be substituted in the wiring scheme layout **110** shown in FIG. **1**A. Among other components, the wiring scheme layout can include, or be used with: a high frequency sensor **22**, a power-line frequency/current sensor **24**, and a differential current sensor **26** which can be a low frequency differential sensor. Generally, sensor **24**, which may function as a current sensor, and differential sensor **26** operate at low frequencies, typically lower than high frequency sensor **22**.

[0043] Any one of the three sensors can each be communicatively arranged and configured to read or measure electrical characteristics of a line or device conductive path such as a phase conductive path or a neutral conductive path. Some of these characteristics can include high frequency signals, current, and current differential on the device current path including one or more of the phase conductive paths and the neutral conductive paths. The term communicatively arranged and configured can result in the positioning of any one of the sensors in any one but not limited to the following configurations: adjacent to the device conductive path, electrically coupled to the device conductive path, magnetically coupled to the device conductive path, positioned such that the device conductive path passes through a core of the sensor.

[0044] For example, high frequency sensor **22** may be configured to read high frequency signals, particularly high frequency noise. Current sensor **24** may be configured to read a current value. Differential sensor **26** may be configured to read a current differential between, e.g., the phase and neutral conductive paths.

[0045] In FIG. **1**A, the output from sensors **22**, **24**, and **26** are connected to circuit **50**. Circuit **50** may be any suitable circuit such as but not limited to an analog signal processor (ASP). This analog signal processor circuit **50** can comprise any suitable circuit elements known in the art such as but not limited to amplifiers, rectifiers, comparators (or a combination thereof), or other elements to condition the signal from one or more of sensors **22**, **24**, and **26** before being input into processor **100**. Alternatively, one or more of the output signals from sensors **22**, **24**, or **26** may be provided directly to processor **100** without any analog conditioning.

[0046] Processor **100** can be any suitable type of processor such as a microprocessor, microcontroller, ASIC, FPGA, or the like. It should also be noted that the term "processor" can be used interchangeably with microprocessor, microcontroller, ASIC, FPGA, or the like.

[0047] Processor **100** is configured or programmed to analyze output signals provided by one or more of sensors **22**, **24**, or **26** and determine if a predetermined dangerous condition exists; e.g., an arc fault, ground fault, or the like. If processor **100** detects a predetermined condition, the processor **100** may be configured or programmed to trigger